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PATENT APPLICATION

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Michael B. Raynham	*Confirmation No.:*
Application No.: 09/430,192	*Examiner:* Tonia L. Meonske
Filing Date: Oct. 29, 1999	*Group Art Unit:* 2183

Title: INTEGRATED MICRO-CONTROLLER AND PROGRAMMABLE LOGIC DEVICE

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith in ***triplicate*** is the Appeal Brief in this application with respect to the Notice of Appeal filed on ***Jan. 21, 2004***.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $320.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( ) one month	$110.00
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( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account ***08-2025*** the sum of ***$320.00***. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

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Signature: _____

Respectfully submitted,

Michael B. Raynham

By _____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicants:	Michael B. Raynham et al.
Application No.:	09/430,192
Filed:	October 29, 1999
Title:	Integrated Micro-Controller and Programmable Logic Device
Examiner:	Tonia L. Meonske
Art Unit:	2183
Docket No.:	10981963-1
Date:	March 22, 2004

BRIEF ON APPEAL

Commissioner of Patents and Trademarks
Washington, DC 20231

Sir:

This appeal is from the decision of the Examiner, in an Office Action mailed on November, 28, 2003, finally rejecting claims 1-10.

REAL PARTY IN INTEREST

Hewlett-Packard Development Company, L.P. is the Assignee of the present patent application. Hewlett-Packard Development Company, L.P., is a Texas corporation with headquarters in Houston, Texas.

RELATED APPEALS AND INTERFERENCES

Applicants' representative has not identified, and does not know of, any other appeals of interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-10 are pending in the application. Claims 1-10 were finally rejected in the Office Action dated November, 28, 2003. Applicants' appeal the final rejection of claims 1-10, which are copied in the attached Appendix I.

STATUS OF AMENDMENTS

No Amendment After Final is enclosed with this brief. The last amendments to the claims were made in the Amendment filed September 5, 2003.

SUMMARY OF INVENTION

Applicants' claims are directed various embodiments of a subsystem controller, an auxiliary processing component used to offload specific processing tasks from system processing components, or central processing units ("CPU"s), implemented as a single integrated circuit that includes a microprocessor, or micro-controller, a complex programmable logic device ("CPLD"), several types of memories, including a random access memory ("RAM") and a read only memory ("ROM"), and several communications interfaces. As discussed in the current application with respect to Figure 1, use of a CPLD and a microprocessor allows a subsystem controller designer to partition logic between circuit-level logic programmed into the CPLD and software routines stored in ROM for execution by the micro-controller. Prior to Applicants' invention, subsystem controllers were implemented as a collection of discrete components mounted to a printed circuit board ("PCB"). There are many reasons why electronics manufacturers neither contemplated nor produced single-integrated-circuit subsystem controllers. Foremost among them is that the various components of Applicants' claimed subsystem controller, including micro-controllers, read-only memories, random-access memories, and complex programmable logic devices, have long been available as discrete, extremely low-cost components. It would have been difficult, prior to Applicants' claimed invention, for an electronics manufacturer to imagine or justify the large design, development, and tooling costs associated with developing and manufacturing a new integrated circuit when these discrete components were already widely and cheaply available. However, a single integrated circuit has many advantages, including low power consumption, reliability, and economic efficiencies, provided that a sufficient market for the single integrated circuit is available to

amortize the huge initial costs of single-integrated-circuit design and development. Unfortunately, subsystem controllers are quite specific for the subsystems that they control, and generally represent markets too small to justify single-integrated-circuit implementations. Applicants realized that, by combining both a CPLD and microprocessor, along with various types of memories and interface, together in a single integrated circuit, they could produce a wide range of subsystem controllers by programming the CPLD in different ways and by including different software routines in the ROM for execution by the microprocessor.

ISSUES

1. Whether a claim is interpreted in accordance with intrinsic evidence, including the specification and definitions included in the specification, and commonly understood definitions of terms, or whether, instead, a claim is interpreted in accordance with definitions proposed by the Examiner.

2. Whether claim 1 is unpatentable under 35 U.S.C. § 103.

3. Whether claims 2-5, that depend from claim 1, are unpatentable under 35 U.S.C. § 103.

4. Whether claim 6 is unpatentable under 35 U.S.C. § 103.

5. Whether claims 7-10, that depend from claim 6, are unpatentable under 35 U.S.C. § 103.

GROUPING OF CLAIMS

Because each of the appealed independent claims 1 and 6 present different facets of the present invention, and because each of the dependent claims introduce additional elements or qualifications, no grouping of the claims naturally appears that requires claims as a group to stand or fall together. Therefore, each of the appealed claims must be considered separately.

ARGUMENT

Claims 1-10 are pending in the current application. In the Office Action dated May 5, 2003, the Examiner rejected claims 1, 2, 4-6, and 8-10 under 35 USC §103(a) as being unpatentable over Wirthlin et al., "The Nano Processor: a Low Resource Reconfigurable Processor" ("Wirthlin") in view of Que's Computer Users Dictionary, Fifth Edition., Pfaffenberger, Brian, 1994 ("Que"), and Page, "Reconfigurable Processors" ("Page"), rejected claim 3 under 35 USC §103(a) as being unpatentable over Sudo, U.S. Patent No. 6,047,198 ("Sudo") in view of Wirthlin, Que, and Page, rejected claim 7 under 35 USC §103(a) as being unpatentable over Sudo in view of Wirthlin and Page, and rejected claims 1-10 under 35 USC §103(a) as being unpatentable over Huffener, U.S. patent No. 5,382,891 in view of Wirthlin. Applicants respectfully disagree with these 35 USC §103(a) rejections.

Issue 1

1. Whether a claim is interpreted in accordance with intrinsic evidence, including the specification and definitions included in the specification, and commonly understood definitions of terms, or whether, instead, a claim is interpreted in accordance with definitions proposed by the Examiner.

A number of claim rejections involve a rather central disagreement between Applicants and the Examiner with respect to the interpretation of the claims. In claims 1-5, Applicants claim a "subsystem controller implemented as a single integrated circuit," and in claims 6-10, Applicants claim a method that includes a step of "providing a single-IC subsystem controller." Applicants' representative has repeatedly called to the Examiner's attention the fact that the term "subsystem controller" is explicitly defined in the current application, and is well-known to those ordinarily skilled in systems design. For example, in the Response filed September 5, 2003, Applicants' representative noted:

> Please note that claim 1 clear claims a subsystem controller that is a separate and distinct entity from a system processor, and please note further that claim 1 is consonant with the definition of a subsystem controller provided in the current application, beginning on line 11 of page 1:
>
> Subsystem controllers are ubiquitous components of modern computer systems, peripheral devices within computer systems, and other electronic devices. The term "subsystem controller" generally refers to a subcomponent of a more complex electronic system, such as a computer, that comprises logic circuits, a

> programmable logic device, and a general-purpose micro-controller that executes a number of software routines. A subsystem controller is generally dedicated to one or a small number of specific control tasks. For example, the control of LED and LCD display devices incorporated in a front panel display of a computer system is generally carried out by one or more subsystem controllers. Use of subsystem controllers may offload computationally intensive and time-intensive tasks from the main processor or processors of computer systems, and may significantly decrease data traffic on critical busses of the computer system that are bottlenecks for data movement within the computer system. (emphasis added)

As another example, Applicants' representative stated, in the Response filed July 24, 2002:

> In The Electrical Engineering Handbook, Dorf, Richard, CRC Press, 1993, page 614, an integrated circuit or IC is defined as: "an assembly of miniature electronic components simultaneously produced in batch processing, on or within a single substrate, which performs an electronic circuit function." In other words, an integrated circuit is what is commonly referred to a chip. A collection of discrete components soldered to, and electronically interconnected by, signal lines on a printed circuit board is not an integrated circuit.
>
> The term "subsystem controller" is well-known in the art. As stated in the Background of the Invention section of the current application, a subsystem controller "is generally dedicated to one or a small number of specific control tasks." (Page 1, lines 16-17). The current application provides several examples, including control of LED and LCD display devices incorporated in a front panel display of the computer system. As is well-known in the art, a controller controls another device through a set of commands that alter the state of the device and direct the device to carry out tasks corresponding to the commands. Additional examples of subsystem controllers include I/O device controllers. In addition to the term "subsystem controller," claim 1 includes an electronic interface element for interfacing the claimed subsystem controller "to a device or subsystem controlled by the subsystem controller." Thus, Applicants' claimed subsystem controller controls a different device or subsystem within an electronic system containing the subsystem controller.

Applicants' explicit definition of the term "subsystem controller" is fully consonant with the ordinary meaning of the individual components of the terms. The term "subsystem" refers to a component or part of a larger system, and the term "controller" refers to something that controls, or controls operation of, another entity. It is manifestly well understood by system designers and manufacturers that subsystem controllers refer to ancillary or auxiliary control components that control devices such as front-panel displays, peripheral devices, etc., within larger systems, such as computer systems, that employ central processing components. By contrast, a well understood definition of the term "CPU" available on the Webopedia web site is:

> Abbreviation of *central processing unit*, and pronounced as separate letters. The CPU is the brains of the computer. Sometimes referred to simply as the *processor* or *central processor*,

> the CPU is where most calculations take place. In terms of computing power, the CPU is the most important element of a computer system.

(http://www.webopedia.com/TERM/C/CPU.html)

The Examiner prefers to interpret the term "subsystem controller" not according to the commonly understood definition of this term, or according to Applicants' explicit definition of the term "subsystem controller," but instead according to the Examiner's own definition of the term. For example, in the Office Action dated November 28, 2003, the Examiner states, in section 10:

> However, the claim language does not exclude the subsystem controller from also being a CPU. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. ... Furthermore, Sudo, in combination with Wirthlin, Que, and Page have taught the CPU, or subsystem controller, provides control for the subsystem.

The Examiner appears to make a similar argument in sections 14 and 15.

The fact that the Examiner can find a reference in which a CPU controls a subsystem does not, in any way, suggest that a CPU is therefore a subsystem controller, according to either the explicit definition of "subsystem controller" provided by Applicants in the specification, or according to the definition of the term "subsystem controller" commonly understood by those skilled in the art. A subsystem controller is generally dedicated to one or a small number of specific control tasks, and offloads computationally intensive and time-intensive tasks from the main processor or processors of computer systems. A subsystem controller may contain a processor, but is not the CPU that is the brains of a computer, where most calculations take place, and that is the most important element of a computer system. Certainly, in lower end computer systems, only a few subsystem controllers may be employed, and the CPU may be tasked with controlling subsystems that would be controlled by subsystem controllers in larger computer systems. But the lower-end-computer-system CPU is not dedicated to one or a small number of specific control tasks, and does not offload computationally intensive and time-intensive tasks from the main processor or processors of computer system. It is, instead, a CPU that, in addition to being the main processor for the system, controls various subsystems. There would logically be no need for the term "subsystem controller" if the term "subsystem controller" were equivalent to the term "CPU."

As is often stated in federal circuit decisions, and as stated in *CCS Fitness Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366, 62 USPQ2d 1658, 1662 (Fed. Cir. 2002):

> Claim interpretation begins with an examination of the intrinsic evidence, i.e., the claims, the rest of the specification and, if in evidence, the prosecution history. Gart v. Logitech, Inc., 254 F.3d 1334, 1339-40, 59 USPQ2d 1290, 1293-94 (Fed. Cir. 2001); O.I. Corp. v. Tekmar Co. Inc., 115 F.3d 1576, 1581, 42 USPQ2d 1777, 1780 (Fed. Cir. 1997). ...
>
> Generally speaking, we indulge a "heavy presumption" that a claim term carries its ordinary and customary meaning. Johnson Worldwide, 175 F.3d at 989, 50 USPQ2d at 1610; accord Gart, 254 F.3d at 1341, 59 USPQ2d at 1295; Kegel, 127 F.3d at 1427, 44 USPQ2d at 1127. ...
>
> Rather, as shown by our precedents, a court may constrict the ordinary meaning of a claim term in at least one of four ways. First, the claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history. E.g., Johnson Worldwide, 175 F.3d at 990, 50 USPQ2d at 1610; Rexnord, 274 F.3d at 1342, 60 USPQ2d at 1854. Second, a claim term will not carry its ordinary meaning if the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention ...

As the above-quoted opinion clearly indicates, an Applicant may indeed define terms in a specification, and use those defined terms in claims to mean what the Applicant has defined them to mean. In the present case, the Applicants' definition of the term "subsystem controller" is equivalent to the definition of subsystem controller commonly understood by those skilled in the art. Similarly, a "subsystem controller implemented as a single integrated circuit" clearly means a subsystem controller implemented as a single chip. In Applicants' opinion, the Examiner is not free to substitute the Examiner's definition of "subsystem controller" and "subsystem controller implemented as a single integrated circuit" for the common understanding of the terms and for Applicants' explicit definition of the terms. Were an Applicant not allowed to depend on such well-defined terms in claim drafting, claims would necessarily become encyclopedic in nature, and cumbersome to the point of incomprehensibility. Reliance on well-defined terms is not only allowable under case law and statue, but a desirable practice, from the standpoint of both clarity and conciseness.

Finally, as clearly stated in the Response filed July 24, 2002:

> In independent claim 1, both the phrases "subsystem controller" and the term "single integrated circuit" clearly represent limitations. In independent claim 6, the phrase "single-IC subsystem controller" occurs repeatedly within the elements of the claim. *In short, Applicants intended to claim in claims 1-10, and did, in fact, clearly claim, a subsystem controller implemented as a single integrated circuit.* This is clear not only from the claim language, but from the specification. In the

> Background of the Invention section of the application, Applicants acknowledge that subsystem controllers that include programmable logic arrays or programmable logic devices and a micro-controller are well-known in the art (current application, page 1, lines 24-27). Applicants clearly did not file the current application with an intent to claim well-known subsystem controllers implemented using discrete components, including programmable logic arrays and micro-controllers. Instead, as clearly stated in the Background of the Invention section of the current application, Applicants and others recognized "a need for a versatile, low-cost, easy programmable, and energy-efficient subsystem controller device that can be programmed for a variety of different applications" (current application, page 4, lines 14-17). Applicants realized, during the inventive process, that, in attempting to meet the above goals of energy efficiency and low costs, a versatile, low-cost, easily programmable, and energy efficient subsystem controller might be obtained by devising a single integrated circuit including the various components listed as elements in claim 1, and then proceeded to design a single-integrated-circuit subsystem controller. In other words, the claimed invention, as is abundantly clear from the contents of the Background of the Invention section of the current application, relates to a single-integrated-circuit, or single-IC, subsystem controller.

In view of the well-understood definition of the terms "subsystem controller" and "single integrated circuit," in view of Applicants' explicit definition of the term "subsystem controller," in view of the dictionary definitions of the terms "CPU" and "single integrated circuit," and in view of Applicants' representatives' statements in the Responses referred to above, Applicants' representative believes that the Examiner's continued insistence on interpreting the claims according to the Examiner's own definitions of terms is improper, and that rejections, based in part or in whole on such improper claim interpretations, are also improper.

Issue 2

2. Whether claim 1 is unpatentable under 35 U.S.C. § 103.

The Examiner rejects claim 1 alternatively by a combination of Wirthlin, Que, and Page and by a combination of Huffener and Wirthlin. Applicants summarize these references below.

Wirthlin

Wirthlin discloses employing a field programmable gate array ("FPGA"), *rather than a standard microprocessor*, to implement a processor. For example, in the first and second paragraphs of section 3, on page 2, Wirthlin discloses:

> The Nano Processor (nP) is a stored-program processor that achieves application-specific performance with general purpose programmable control. The nP implements application-specific functionality through the development of custom instructions. An integrated assembler generates the program data necessary to convert custom assembly instructions into executable code.
>
> Similar to the Reconfigurable Microprocessor[6], the nP implements the processor control within a FPGA instead of using a standard microprocessor. (emphasis added)

In the Abstract, Wirthlin describes:

> One way to introduce a more flexible development approach is to implement a customizable stored-program processor. For a given application, the designer can develop customized hardware to increase performance and then control the sequencing and operation of this hardware with software.

It may be possible to argue that Wirthlin discloses a FPGA implementation of a processing component. Alternatively, it may be possible to argue that Wirthlin discloses a stored-program micro-controller. However, Wirthlin does not disclose an implementation that includes both a CPLD, with programmed, control logic circuits, and a micro-controller that executes control software routines. In essence, Wirthlin discloses a micro-controller implemented by a FPGA.

Que

Que is a dictionary entry defining the term "read-only memory" that describes a trend of storing portions of an operating system on ROM chips instead of on disk. Que makes it clear that these portions of the operating system are startup instructions and functions, needed to bootstrap a computer system:

> Because the computer's random-access memory (RAM) is volatile (loses information when you switch off the power), the computer's internal memory is blank at power up, and the computer can perform no functions unless given startup instructions. These instructions are stored in ROM. A growing trend is toward including substantial portions of the operating system on ROM chips instead of on disk.

Que discusses computer systems, and discusses discrete RAM and ROM chips within a computer system. Que does not suggest including either RAM or ROM within a processor, or within any kind of integrated circuit that includes functionality other than memory.

Page

Page discloses combining a processor and a dynamically programmable gate

array within a single integrated circuit. Page is, however, clearly concerned with implementing CPUs, not subsystem controllers. For example, Page argues, in the second paragraph on page 1, that:

> conventional microprocessors are a poor match for any *particular* application, though they support a wide range of applications well. We suggest that the solution is to use additional silicon to provide hardware which can be configured to support any application. By combining a conventional processor with a DPGA on a single chip, commodity pricing is maintained and yet the same part can be targeted effectively across a wide range of applications.

Subsystem controllers do not run applications, i.e. computer application programs, and certainly do not run *any* applications. Page is clearly proposing a type of general purpose CPU – not a subsystem controller. Later, Page states:

> However, there is scope for real technical innovation since there is no longer the same necessity to regard the processor core as sacrosanct and we can consider making changes to it as well as to the DPGA so that the combination becomes even better at supporting user applications. (emphasis added)

Page essentially alludes to a single-integrated-circuit CPU containing a dynamically programmable gate array ("DPGA") and a microprocessor, and nothing more. Page does not suggest including additional components in the single-integrated-circuit CPU, nor employing the single-integrated-circuit CPU as a subsystem controller.

Huffener

Huffener discloses a mechanical and motorized foot pedal that interfaces with a network for sequencing music and multi-media data (Huffener, abstract). The Examiner states, in section 22 of the Office Action dated May 5, 2003, that "Huffener has taught a subsystem controller implemented as a single integrated circuit for control of a device or subsystem within an electronic system having system processing components (Figure 12)." A cursory review of Figure 12 reveals a quite contrary implementation. As discussed beginning on line 9 of column 10 of Huffener, the logic circuit shown in Figure 12 includes discrete encoders 94 and 95 interfaced with a discrete "8-bit single chip microcontroller" 85, an EPROM 87, an optical coupler 93, an 8-bit latch 88, a digital/analog converter 89, and numerous other components. A logic circuit that includes a discrete "8-bit single chip microcontroller" to which other components interface is not a single integrated circuit. Huffener is a simple musical-system device that includes a discrete microprocessor, as do so

many currently-available devices.

Claimed Subject Matter

Consider the invention claimed in claim 1, with numerical annotations and emphasis added to point out particular elements and claim language:

> 1. A *(1)* subsystem controller *(2)* implemented as a single integrated circuit *(3)* for control of a device or subsystem *(4)* within an electronic system having system processing components, the subsystem controller comprising:
>
> *(5)* a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality;
>
> *(6)* a micro-controller that can execute software routines that implement control functionality;
>
> *(7)* read-only memory that stores executable code for execution by the micro-controller;
>
> *(8)* random-access memory that can store data and executable code for execution by the micro-controller;
>
> *(9)* a bus interface for exchanging data and control signals between the subsystem controller and system processing components; and
>
> *(10)* an additional electronic interface to a device or subsystem controlled by the subsystem controller. (emphasis and parenthesized numerals added)

In particular, the claimed invention is a subsystem controller, the term "subsystem controller" both explicitly defined in the current application and having a well-known meaning to those ordinarily skilled in the art of system design and manufacture, as discussed above with respect to Issue 1. Moreover, the claimed subsystem controller is implemented as a single integrated circuit, also discussed.

Prima Facie Case of Obviousness

According to the MPEP §2143:

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In particular, each element of the claim must be taught or suggested, and a teaching or

suggestion for the combination must be found in the prior art.

Comparison of the Claimed Invention With the Combinations of Wirthlin, Que, and Page and Huffener and Wirthlin

In order to facilitate a comparison of the two combinations with the claimed invention, a table is provided below, each row corresponding to an element or claim language feature of claim 1, numerically identified above, and showing whether or not that element, alone, is taught or suggested in each of the four references of the two combinations:

Element	Wirthlin	Que	Page	Huffener
(1)	yes	no	no	no
(2)	no	no	yes	no
(3)	yes	no	no	no
(4)	yes	yes	yes	yes
(5)	yes	no	yes	no
(6)	no	yes	yes	yes
(7)	no	yes	no	yes
(8)	yes	yes	yes	yes
(9)	yes	no	yes	no
(10)	yes	no	yes	yes

With regard to the first combination of Wirthlin, Que, and Page, it can be seen, in the above table, that each element is taught or suggested in at least one of the three references. However, to make a *Prima Facie* case of obviousness, the Examiner must show a teaching or suggestion for a combination of elements equivalent to the claimed invention.

Consider first that neither Wirthlin nor Page teach, mention, or suggest employing ROM memory. In section 5 of the Office Action of May 5, 2003, the Examiner states that:

> Wirthlin et al. have not taught read-only memory that stores executable code for execution by the micro-controller. However, Que has taught utilizing ROM in place of the random-access memory (RAM) to store executable code to be run on the micro-controller would have allowed for the system to retain such code in the system power-off state and load the code immediately upon a change to power-up (Que page 416). Therefore, it would have been obvious to a person of ordinary skill in the art at the

> time the invention was made to utilize read-only memory, or ROM, to store executable code for execution by the micro-controller as taught by Que instead of the random-access memory, or RAM, of Page, in order to ensure immediate loading of the code upon system power-up.

However, Que does not once mention micro-controllers. Que does mention that there is a growing trend toward storing substantial portions of an operating system on ROM chips, with the caveat that *upgrading ROM is more difficult and expensive than supplying new disks.* (Que, page 416) By contrast, Wirthlin discloses *reconfigurable* logic systems that provide a *flexible* development approach by implementing customizable stored-program processors. (Wirthlin, abstract and title). A component that is difficult and expensive to upgrade would hardly be a likely candidate for a flexible and reconfigurable system. Nowhere does Wirthlin mention or suggest a need to ensure immediate loading of code upon system power-up. Similarly, Page discloses an implementation of a reconfigurable processor (*see* Page, title, subsection headings, figure captions, etc.). Page nowhere mentions or suggests a need to ensure immediate loading of code upon system power-up. As with Wirthlin, component that is difficult and expensive to upgrade would hardly be a likely candidate to include in Page's reconfigurable processor, particular with no apparent need to ensure immediate loading of code upon system power-up. It should also be noted that Que does not once suggest incorporation of ROM in a single integrated circuit with a micro-controller or any other processing component. Que simply mentions that discrete ROM chips are being used to store operating system code in computer systems. The Examiner has failed to provide a credible motivation for the combination of Que with either Wirthlin or Page, and has failed to provide a teaching or suggestion for the combination in the prior art.

Consider next that neither Wirthlin nor Page teach or suggest a single-integrated-circuit implementation of a subsystem controller. Page does teach a single-integrated-circuit implementation of a general processor, or CPU, containing both a microprocessor and a complex programmable logic device. In section 6 of the Office Action of May 5, 2003, the Examiner states that:

> Wirthlin et al. have also not taught that the subsystem controller is implemented as a single integrated circuit. However, Page has taught that combining a programmable logic device and the processor on the same chip reduces the number of parts in a typical system and speeds up system communication . . . It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the subsystem controller, as taught by Wirthlin et al., be implemented as an integrated circuit in order to speed up communication and reduce the number of parts, which reduces the cost of the overall system.

Wirthlin does not once mention or suggest a need for decreasing the number of system parts and speeding up system communication. Indeed, decreasing the number of system parts is not generally a consideration for a *subsystem* controller, which by its very nature increases the number of system parts by introducing an auxiliary processing component, and speeding up *system* communication is not generally within the purview of a *subsystem* controller, except by offloading communications tasks from the system processor. Page's combination of a microprocessor and DPGA on a single chip is motivated by speeding up communications between the DPGA and microprocessor (see quote directly below) but not speeding up any other type of communications. In essence, this is a speed-up of communications between types of components that occur together in Applicants' claimed invention, and not a speed up of communications of a system that contains the single-chip. In other words, the speed-up obtained would speed up communications within a subsystem controller, but there is no indication in Wirthlin, in any other cited reference, or in the current application that there are communications bottlenecks or deficiencies within subsystem controllers.

Of particular note is that Page does not teach or suggest including memory of any kind in a single-integrated-circuit implementation. Instead, Page merely states that:

> If our predictions about the relevance of DPGA co-processors prove to be correct, *then there will soon follow a commodity market for a DPGA and processor on the same chip*. This will obviously yield a reduction in the number of parts in a typical system implementation, and it will also *speed up communication between the two processors*, and may also simplify the communication and clocking arrangements. By this stage of evolution the problems of DPGA-processor interaction will have been characterized across a wide range of real-world applications. *Consequently, simply combining the two elements on a single chip is economically interesting but straightforward in a technical sense, and will not be considered further here.* (Page, page 6, section 6) (emphasis added).

The above-quoted paragraph is the total disclosure in Page related to the current application. Page suggests combining a DPGA and microcontroller in a single integrated circuit, but nothing more. In particular, there is no suggestion for including, in a single integrated circuit, the remaining components listed as being included in Applicants' claimed subsystem controller of claim 1, including: (1) read-only memory that stores executable code for execution by the micro-controller; (2) random-access memory that can store data and executable code for execution by the micro-controller; (3) a bus interface for exchanging data and control signals between the subsystem controller and system processing components; and (4) an additional electronic interface to a device or subsystem controlled by the subsystem controller. At best, Page suggests combining a DPGA and microprocessor together in a

single-integrated-circuit implementation of a CPU. Not one cited reference teaches, mentions, or suggests including anything close to all of the elements of claim 1 in a single integrated circuit, and not one cited reference teaches, mentions, or suggests employing a single-integrated-circuit as a subsystem controller. The combination of elements of claim 1 is simply not suggested by any combination of the cited references.

The Examiner's final statement – that an integrated-circuit-implementation of a subsystem controller reduces the cost of the overall system is not at all obvious. In fact, design and initial manufacture of an integrated-circuit-implementation of a subsystem controller is prohibitively expensive, unless, as recognized by Applicants, the huge cost of an integrated-circuit design an initial manufacture is offset by wide use for controlling many different types of subsystems. As Applicants state in the last paragraph on page 5, continuing to page 6, of their Response of July 24, 2002:

> Prior to Applicants' claimed invention, Applicants' representative can think of no example of a subsystem controller implemented as a single integrated circuit. In fact, there are many reasons why electronics manufacturers neither contemplated nor produced single-integrated-circuit subsystem controllers. First, the discrete components listed in claim 1, including micro-controllers, read-only memories, random-access memories, and complex programmable logic devices, have long been available as discrete, extremely low-cost components. It would have been difficult, prior to Applicants' claimed invention, for an electronics manufacturer to imagine or justify the large design, development, and tooling costs associated with developing and manufacturing a new integrated circuit when these discrete components were already widely and cheaply available. In fact, as far as Applicants' representative knows, no single-integrated-circuit subsystem controllers were manufactured prior to Applicants' claimed invention.

As stated in *In re Dembiczak*, 175 F.3d 994, 998, 50 USPQ 1614, 1616 (Fed. Cir. 1999):

> Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references. See, e.g., C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998) ... Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight. See, e.g., Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed. Cir. 1985) ("The invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time."). In this case, the Board fell into the hindsight trap.
>
> We have noted that evidence of a suggestion, teaching, or motivation to combine may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved, see Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 USPQ2d 1626,

> 1630 (Fed. Cir. 1996), Para- Ordinance Mfg. v. SGS Imports Intern., Inc., 73 F.3d 1085, 1088, 37 USPQ2d 1237, 1240 (Fed. Cir. 1995), although "the suggestion more often comes from the teachings of the pertinent references," Rouffet, 149 F.3d at 1355, 47 USPQ2d at 1456. The range of sources available, however, does not diminish the requirement for actual evidence. That is, the showing must be clear and particular. See, e.g., C.R. Bard, 157 F.3d at 1352, 48 USPQ2d at 1232. Broad conclusory statements regarding the teaching of multiple references, standing alone, are not "evidence."

In Applicants' representative's opinion, the Examiner's stated suggestions for the combination of Page and Wirthlin represent both unsupported conclusory statements, generally inaccurate and not applicable to the current invention, followed by a statement best characterized as hindsight recognition. Designing and initially manufacturing an integrated circuit is an extremely time consuming and expensive task. One of Applicants' most important and inventive realizations was that this high cost could be amortized over many different types of subsystem controllers if the single-integrated-circuit implementation provided the flexibility for application of the single-integrated-circuit implementation to control of many different types of subsystems. It was precisely the cost that steered subsystem controller implementations away from single-integrated-circuit implementations up until the time of Applicants' invention.

Wirthlin does not employ a micro-controller, but instead employs one or more FPGAs. For example, in Figure 7, Wirthlin shows two Xilinx FPGAs, memory, and interfaces. A micro-controller is, as manifestly made clear in the current application (*see*, e.g., the discussion of Figure 1 in the paragraph beginning on line 24 of page 1) a microprocessor that is controlled by software programs, as opposed to a complex programmable logic device or FPGA. Applicants employ a partitioning of control logic between firmware encoded in a CPLD and software running on a microprocessor, or micro-controller. Therefore, a suggestion needs to be found in the prior art not only for combining Wirthlin's subsystem controller with a single-integrated-circuit implementation, as taught by Page for a DPGA/microprocessor-based CPU, but also a combination of a microprocessor/CPLD implementation for a subsystem controller. Page does not teach, suggest, or mention subsystem controllers. The idea for employing a microprocessor/CPLD implementation for a subsystem controller is, as discussed above, an important aspect of Applicants' invention, and the Examiner's finding suggestions for that idea by combining disparate references constitutes hindsight recognition of the invention based on the current application.

The second rejection of claim 1 over Huffener in view of Wirthlin is unsupportable. Neither Huffener nor Wirthlin teach, mention, or suggest a single-integrated-circuit implementation of a subsystem controller, or of anything else other than a discrete FPGA and a discrete microprocessor – both well known in the art. The Examiner states, in section 22 of the Office Action dated May 5, 2003, that "Huffener has taught a subsystem controller implemented as a single integrated circuit." Instead, Huffener has taught the use of a microcontroller (85 in Figure 12), or microprocessor, for executing software stored in a ROM (87 in Figure 12) to carry out the various logic functions of a foot-pedal device (Huffener, column 10, lines 9-27). Figure 12 clearly shows discrete components interconnected, and Huffener refers to the components as discrete, for example, stating that "output of the 8 bit single chip microcontroller (85) is supplied to the motor ..." (Huffener, column 10, lines 43-45). Furthermore, Huffener does not teach, mention, or suggestion a subsystem controller, according either to the above-quoted definition of the term "subsystem controller" explicitly included in the current application, or according to claim 1, which includes "a bus interface for exchanging data and control signals between the subsystem controller and system processing components." There are no system processing components in Huffener's foot pedal other than the microprocessor (85 in Figure 12), which therefore, by definition, and by the language of claim 1, cannot be a subsystem controller. Huffener is completely unrelated art. Standard, discrete-component implementations of the control logic of a device, such as a foot pedal, are not a subsystem controller that is "a subcomponent of a more complex electronic system, such as a computer, that comprises logic circuits, a programmable logic device, and a general-purpose micro-controller and that executes a number of software routines," and that "is generally dedicated to one or a small number of specific control tasks" and having "*a bus interface for exchanging data and control signals between the subsystem controller and system processing components*."

There is not teaching or suggestion in the prior art for combing a standard implementation of a foot-pedal device with Wirthlin's discrete-component, FPGA-based implementation of a subsystem controller to produce Applicants' claimed microprocessor/CPLD-based, single-integrated-circuit implementation of a subsystem controller. Even were a suggestion to be found, the combination does not teach, mention, or suggest Applicants' claimed microprocessor/CPLD-based, single-integrated-circuit implementation of a subsystem controller.

Issue 3

3. Whether claims 2-5, that depend from claim 1, are unpatentable under 35 U.S.C. § 103.

Claims 2-5 depend from claim 1. As discussed above, claim 1 is not obvious in view of a combination of Wirthlin, Que, and Page or a combination of Huffener and Wirthlin. Claims 2-5 are also not obvious in view of these combinations, since they include the language of claim 1. In addition, the Examiner's specific rejections of claims 2-5 include many incorrect statements.

In section 7 of Office Action dated May 5, 2003, the Examiner states that Wirthlin teaches "the subsystem controller of claim 1, as described above, and wherein control functionality of the subsystem controller is partitioned between logic circuits programmed into the complex programmable logic device and software routines executed by the micro-controller (Wirthlin et al., page 2, section 2.2)" Instead, Wirthlin teaches "mixing a stored-program architecture with reconfigurable logic by programming a complex programmable logic device, in Wirthlin's case a field programmable gate array, to act as a stored-program processor. Wirthlin does not employ microprocessors, but instead employs FPGAs programmed to act as microprocessors. However, as clearly stated in the current application, and as clearly claimed in claim 2, Applicants disclose and claim a subsystem controller of "wherein control functionality of the subsystem controller is partitioned between logic circuits programmed into the complex programmable logic device and software routines executed by the micro-controller." Applicants' single-integrated-circuit subsystem controller includes a microprocessor and a CPLD, and partitions control logic implementation between the two. Wirthlin's disclosed devices include only FPGAs.

In specifically rejecting claim 3, in section 10 of Office Action dated May 5, 2003, the Examiner cites Sudo. Sudo is completely unrelated art. Sudo discloses a communications terminal in which a CPU (7 in Figure 4) controls "the LCD 5 via a liquid display driver 5A and displays various types of information ..." and controls "a sending/receiving circuit section and sends and receives various types of information .." (column 4, lines 13-20). As is clearly shown in Figure 4, the CPU in Sudo is a discrete component, and controls all logic functions within the communications terminal. Sudo, like Huffener, has nothing at all to do with subsystem controllers, which, as explicitly defined in the current application and as well-understood by systems designers, are special-purpose, auxiliary processors that perform one or a few specific control tasks to offload processing

from the central processors of a computer system and decrease bandwidth requirements of CPUs communicating with peripheral components. The Examiner continues to maintain that Sudo is relevant, arguing in section 14 of the Office Action of November 28, 2003 that a combination of Sudo and Wirthlin, in which Wirthlin's FPGA-based subsystem controller inserted into Sudo's communication terminal, produces a relevant subsystem controller. Insertion of Wirthlin's FPGA-based device into Sudo in place of Sudo's CPU produces a communications terminal controlled by an FPGA-based CPU device – not a subsystem controller. A subsystem controller is an auxiliary processor, as explicitly defined in the current application and as explicitly claimed in claim 1, from which claim 3 depends. To obtain a subsystem controller, Wirthlin's device would need to be added to Sudo's device to control the LCD display. But there is no teaching or suggestion in Sudo, Wirthlin, or any other reference for adding a complex and expensive component to a simple device which does not need it. Sudo's CPU has more than adequate processing capability to control the LCD and communications components. Any currently available microprocessor would have adequate processing power. The expense and added complexity of a subsystem controllers can be justified only in a computer system, or other complex system, in which significant CPU resources needed for computational tasks are diverted for controlling peripheral devices and other subcomponents. Sudo shows only two subcomponents requiring control, and describes no general computational tasks. Sudo's device simply has no need for a subsystem controller, and there is no suggestion in the cited references or in the general knowledge for including one in Sudo communications terminal.

The Examiner relies on no additional references in the first set of rejections of claims 2-5 other than Sudo. No combination of Wirthlin, Page, Que, and Sudo produces the claimed single-integrated-circuit implementation of a subsystem controller containing both a microcontroller and a CPLD. The second set of rejections of claims 2-5 based on a combination of Huffener's foot-pedal device and Wirthlin's CPLD-based subsystem controller fail for the same reasons that a combination of Huffener's foot-pedal device and Wirthlin fail to make claim 1 obvious. Neither Huffener nor Wirthlin disclose a single-integrated-circuit implementation, and there is no teaching or suggestion for combining a simple foot-pedal device controlled by a microcontroller with a CPLD-based subsystem controller.

Issue 4

4. Whether claim 6 is unpatentable under 35 U.S.C. § 103.

Claim 6 is a method claim directed to controlling a subsystem within a complex electrical device, and includes elements of "providing a single-IC subsystem controller", "programming logic circuits into a complex programmable logic device included in the single-IC subsystem controller," " implementing software routines for execution by a micro-controller within the single-IC subsystem controller," and "storing the software routines in the single-IC subsystem controller." In the Office Action of May 5, 2003, the Examiner rejects claim 6 over a combination of Wirthlin, Que, and Page. Applicants disagree with this rejection for the same reasons as Applicants disagree with the similar rejection of claim 1. Page does not teach, mention, or suggest a subsystem controller implementation, and does not suggest incorporation of any kind of memory for storing programs in a single-integrated-circuit implementation, as discussed above with respect to the rejections of claim 1. Page in no way motivates or suggests use of a combined CPLD/microprocessor implementation as a subsystem controller. Page is directed to implementation of CPUs for executing specific computer application programs. (Page, page 2, section 3). Wirthlin discloses reconfigurable devices using CPLDs, but not microprocessors, and suggests no single-integrated-circuit implementation of any kind. Que is a dictionary reference defining the term ROM, and suggests that ROM is relatively difficult to upgrade and expensive – certainly no suggestion for including ROM in a reconfigurable processor as described by both Wirthlin and Page. The combination of Wirthlin, Que, and Page do not teach, mention, or suggest the claimed method, and there is absolutely no suggestion for the combination in Wirthlin, Page, and Que, nor in the knowledge of those skilled in the art of systems design and subsystem controllers.

Claim 6 is not obvious over a combination of Wirthlin and Huffener, as neither teaches, mentions, or suggests a single-integrated-circuit implementation of anything, let alone a subsystem controller. Additional arguments against the Wirthlin/Huffener combination are included above, with respect to issue 2.

5. Whether claims 7-10, that depend from claim 6, are unpatentable under 35 U.S.C. § 103.

Claims 7-10, which depend from independent claim 6, are nonobviousness for

the same reasons that claim 6 and claims 1-5 are nonobvious. There is no combination of two or more of Wirthlin, Que, Page, Sudo, and Huffener that teaches or suggests the claimed method. There is no suggestion in the references, or within the knowledge of those skilled in the art, for the combinations employed by the Examiner in the obviousness rejections.

CONCLUSION

Applicants' representative stated, in the Response of September 5, 2003:

> Had a single-IC implementation of a subsystem controller been obvious in view of the cited references, it would nothing short of astonishing that, by October 1999, in an extremely competitive, subsystem-controller commodity market, not one such implementation was available, produced, prototyped, described, or proposed. Applicants believe that without a clear showing of an explicit or implicit suggestion for a single-IC implementation of a subsystem controller, containing the claimed subsystem-controller elements, an obviousness-type rejection is not sustainable.

In the Office Action of November 28, 2003, the Examiner responded:

> Applicant appears to be stating that the claimed subject matter solved a problem that was long standing in the art. However, there is no showing that others of ordinary skill in the art were working on the problem and if so, for how long. In addition, there is no evidence that if persons skilled in the art who were presumably working on the problem knew of the teachings of the above cited references, they would still be unable to solve the problem.

Applicants' representative appreciates that Examiner's attention to evidentiary requirements, and acknowledges not having specifically included evidence in support of the above statement. Of course, because the Applicants' invention provides an unanticipated breakthrough in subsystem controller design, it would be difficult to show that others were working on the same problem. Certainly, others were working on designing subsystem controllers, including, apparently, Wirthlin. Applicants' representative did not include "evidence that if persons skilled in the art who were presumably working on the problem knew of the teachings of the above cited references, they would still be unable to solve the problem," because the teachings of the above cited references do not, alone or in any combination, teach or suggest Applicants' claimed invention, as discussed above. The cited references together merely teach well-known components, such as memories, CPUs, etc., with one reference teaching a DPGA/microprocessor combination for use as a CPU, and another reference teaching implementing a type of subsystem controller using discrete FPGAs. There is no suggestion for combining the components of Applicants' claimed subsystem controller together in a single integrated circuit and using the single integrated

circuit as a subsystem controller. In essence, the cited references would not point one ordinarily skilled in the art in the direction of Applicants' invention.

By the same token, in four Office Actions, the Examiner has not been able to provide a combination of references that teach or suggest Applicants' claimed invention, and has not been able to find any reference for a single-integrated-circuit implementation of a subsystem controller. Applicants' representative continues to believe that, in a very crowded art field, the lack of any cited reference teaching or suggesting the claimed invention, or any combination of references teaching or suggesting the claimed invention, is a very strong indication of the nonobviousness of Applicants' claimed invention.

Applicant respectfully submits that all statutory requirements are met and that the present application is allowable over all the references of record. Applicants do not believe that further prosecution will produce any additional references that alone, or in combination, will come any closer to providing a reasonable basis for an obviousness-type rejection than those already provided by the Examiner. Therefore, Applicant respectfully requests that the current application be passed to issue.

Respectfully submitted,
Michael B. Raynham et al.
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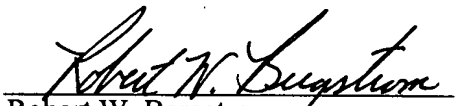
By 
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circuit as a subsystem controller. In essence, the cited references would not point one ordinarily skilled in the art in the direction of Applicants' invention.

By the same token, in four Office Actions, the Examiner has not been able to provide a combination of references that teach or suggest Applicants' claimed invention, and has not been able to find any reference for a single-integrated-circuit implementation of a subsystem controller. Applicants' representative continues to believe that, in a very crowded art field, the lack of any cited reference teaching or suggesting the claimed invention, or any combination of references teaching or suggesting the claimed invention, is a very strong indication of the nonobviousness of Applicants' claimed invention.

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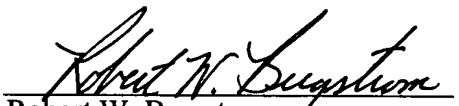
By 
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APPENDIX I

1. A subsystem controller implemented as a single integrated circuit for control of a device or subsystem within an electronic system having system processing components, the subsystem controller comprising:

a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality;

a micro-controller that can execute software routines that implement control functionality;

read-only memory that stores executable code for execution by the micro-controller;

random-access memory that can store data and executable code for execution by the micro-controller;

a bus interface for exchanging data and control signals between the subsystem controller and system processing components; and

an additional electronic interface to a device or subsystem controlled by the subsystem controller.

2. The subsystem controller of claim 1 wherein control functionality of the subsystem controller is partitioned between logic circuits programmed into the complex programmable logic device and software routines executed by the micro-controller.

3. The subsystem controller of claim 1 programmed to control display of information on an LCD display window included in an external front panel display of a server computer.

4. The subsystem controller of claim 1 wherein the bus interface is an I^2C bus interface.

5. The subsystem controller of claim 1 wherein the additional electronic interface is an 8-bit input/output bus and additional signal lines.

6. A method for controlling a subsystem within a complex electrical device, the method comprising:

providing a single-IC subsystem controller;

programming control functionality into the single-IC subsystem controller by

programming logic circuits into a complex programmable logic device

included in the single-IC subsystem controller,

implementing software routines for execution by a micro-controller within the single-IC subsystem controller, and

storing the software routines in the single-IC subsystem controller; and

interconnecting the single-IC subsystem controller to the subsystem within the complex electrical device.

7. The method of claim 6 wherein the subsystem is an LCD display window that displays information about the components within the complex electrical device and about the state of the complex electrical device.

8. The method of claim 6 wherein the complex electrical device is a computer system.

9. The method of claim 6 wherein the single-IC subsystem controller includes the complex programmable logic device, the micro-controller, a read-only memory, a random-access memory, a bus interface, and an additional electronic interface.

10. The method of claim 9 wherein interconnecting the single-IC subsystem controller to the subsystem within the complex electrical device further includes interconnecting the subsystem with the additional electronic interface.